IN THE CLAIMS

Please amend the claims as follows:

Claims 1-13 are withdrawn from consideration.

14. (Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more gates are of a predetermined width and length at a substantially identical gap between ones of the adjacent transistor gates on the substrate; and

a plurality of dummy gates having predetermined width and length between ones of the adjacent transistors at a substantially identical gap between adjacent ones of the dummy gates as that between the adjacent ones of the transistor gates on the substrate.

15. (Amended) The device, as defined in claim 14, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

16. The device, as defined in claim 14, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

17. The device, as defined in claim 14, wherein a plurality of dummy gates are commonly connected on the substrate.

18. (Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate is of predetermined width and length at a substantially identical gap between adjacent ones of the transistor gates on the substrate; and

a plurality of dummy gates having predetermined width and length between and outside ones of the adjacent transistors at a substantially identical gap between adjacent ones of the dummy gates as that between the adjacent ones of transistor gates on the substrate.

19. (Amended) The device, as defined in claim 18, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

20. The device, as defined in claim 18, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

21. The device, as defined in claim 18, wherein a plurality of dummy gates are commonly connected on the substrate.

22. (Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate has a predetermined width and length at a substantially identical gap between ones of the adjacent gates on the substrate; and

a plurality of dummy gates having predetermined width and length outside ones of the adjacent transistors at a substantially identical gap between adjacent ones of the dummy gates as that between the adjacent ones of the transistor gates on the substrate.

23. The device, as defined in claim 22, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

24. The device, as defined in claim 22, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

25. The device, as defined in claim 22, wherein a plurality of dummy gates are commonly connected on the substrate.

26. Cancel claim.

27. Cancel claim.

28. Cancel claim.

29. (New) A semiconductor device comprising:

a substrate;

active regions having a source region and a drain region on the substrate;

a portion other than the active region on the substrate;

a plurality of transistor gates formed on the active regions, the gates being disposed between the source region and the drain region and having a first gap between adjacent gates;

a plurality of dummy gates formed on the portion, the dummy gates being characterized by a second gap between adjacent dummy gates;

wherein the second gap is substantially identical to the first gap.

30. (New) The device, according to claim 29, in which a first metal is connected to the source region and the drain region by a plurality of contacts.

31. (New) The device, according to claim 30, in which a second metal is connected to a first part of the first metal to supply a voltage.

32. (New) The device, according to claim 31, in which the plurality of dummy gates are commonly connected by a second part of the first metal to supply a ground voltage.

33. (New) A semiconductor device comprising

a substrate;

a first region having a plurality of first active regions each having a source region and a drain region respectively and a first portion other than the plurality of first active regions on the substrate;

a second region having a plurality of second active regions each having a source region and a drain region respectively and a second portion other than the plurality of second active regions on the substrate;

a plurality of first transistor gates formed on the plurality of first active regions, disposed between the source region and the drain region, the plurality of first gates being characterized by a first gap between neighboring transistor gates;

a plurality of second transistor gates formed on the plurality of second active regions, the plurality of second gates also being characterized by the first gap between neighboring gates;

a plurality of first dummy gates formed on the first portion, the plurality of first dummy gates being characterized by a second gap between neighboring dummy gates;

a plurality of second dummy gates formed on the second portion, the plurality of second dummy gates also being characterized by the second gap between neighboring dummy gates;

a first metal connected to the source and drain regions by a contact; and

a second metal connected to a first part of the first metal to supply a voltage.

34. (New) The semiconductor device according to claim 33, in which the first gap is substantially identical to the second gap.

35. (New) The semiconductor device according to claim 33, in which the second metal is connected to a second part of the first metal to supply a ground voltage.

36. (New) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions, the plurality of transistor gates being characterized by a predetermined first dimension and a variable second dimension on the substrate; and

a plurality of dummy gates disposed on the substrate between more than one first and second electrodes of those active regions, the plurality of dummy gates being characterized by dummy gates that substantially fill the region on the substrate devoid of transistor gates in the second dimension;

wherein the plurality of transistor gates have substantially identical first and second dimensions.

37. (New) The semiconductor device according to claim 36, in which the first dimension characterizes a transistor gate length.

38. (New) The semiconductor device according to claim 37, in which the second dimension characterizes a transistor gate width.

39. (New) The semiconductor device according to claim 38, in which adjacent ones of the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates.